



Dr. M.G.R. EDUCATIONAL AND RESEARCH INSTITUTE (Deemed to be University)

Maduravoyal, Chennai - 600 095. Tamilnadu, India.

(An ISO 9001-2015 Certified Institution)



MGR ASSOCIATION FOR GREAT INNOVATIVE CREATORS

Department of Electronics and Communication Engineering

Event Title	Certificate Training Program on "Verilog for a FPGA Engineer with Xilinx Vivado Design suite"		
Objective of Event	Students gained foundational knowledge and hands-on experience in FPGA design and Verilog programming, successfully implemented combinational logic circuits, and explored real-world applications like image processing, enhancing their readiness for VLSI projects.		
Chief Guest /Speaker Details	Mr.K.A. Vinnalan, Application Engineer, , CoreEL Technologies		
Date	19/08/2024 to 23/08/2024	Time	02.00 PM to 04.00 PM
Venue	VLSI Lab	No. of Participants	70

REPORT

TITLE

Certificate Course on Verilog for a FPGA Engineer with Xilinx Vivado Design suite

CONTENT

The course is aimed to impart knowledge on the topics of FPGA architecture and verilog programming on Xilinx Vivado design suite. Fifty third year students were selected for the 5 days training programme. The first day session was started with a topic of "Introduction to VLSI" by Ms. G.Jegadeesari, A.P, ECE Department, Dr. MGR Educational and Research Institute at 2 pm on 19th August 2024. The second session on the same day was delivered by Dr.V.Amudha, on the topic "Introduction to Verilog Programming". The students did programming for basic logic gates on Vivado design suite. On the second day 20th aug 2024, Dr. G. Themozhi, Professor, ECE delivered a lecture on the topic "Verilog Gate level modeling" followed by the Vivado project flow explained by. Dr. Anandhi, Associate Professor, ECE.

On the third day 21st aug,2024,Mr.K.A. Vinnalan, Application Engineer, CoreEL Technologies, Chennai elaborated on FPGA implementation of half adder with a demonstration using Zynq FPGA board. Participants able to simulate combinational logic circuits using Vivado software. During the 4th day 22nd Aug 2024, on Mr K.A. Vinnalan elaborated different Xilinx FPGA families for different applications and also demonstrated with image processing application on Zynq board. The students interacted with him with many questions and it will be a foundation platform for their VLSI projects.

On 23rd Aug, 2024, Ms. Jegadeeswari delivered a lecture on Verilog Behavioral



Dr. M.G.R.
EDUCATIONAL AND RESEARCH INSTITUTE
(Deemed to be University)
Maduravoyal, Chennai - 600 095. Tamilnadu, India.
(An ISO 9001-2015 Certified Institution)



MGR ASSOCIATION FOR GREAT INNOVATIVE CREATORS

modeling programming for multiplexers and Arithmetic Logic Units. Followed by the session Dr.V.Amudha discussed with a topic of Speech Recognition on System on Chip application. The training programme came to end with students interactions and feedback.



EVENT OUTCOME

The 5-day training aimed to introduce third-year students to FPGA architecture and Verilog programming using the Xilinx Vivado Design Suite, providing both theoretical knowledge and practical skills.

PHOTOS

Dr. M. Kumaresan/ Dr. Amutha