Department of Electronics and Communication Engineering			
Event Title	FDP on " VLSI design "		
Objective of Event	To understand the basics of VLSI Design		
Chief Guest /Speaker Details	PROF.DR.USHAA ESWARAN, Principal & Professor – Dept. of ECE,, Indira Institute of Technology and Science		
Date	18/12/2023 to 24/12/2023	Time	10.00AM to 1.00PM
Venue	Google Meet	No. of Participants	60

REPORT

TITLE

FDP on " VLSI design "

CONTENT

Day1: Empowering ECE Faculty in VLSI Design

On December 18, 2023, the Department of Electronics and Communication Engineering (ECE) commenced a six-day faculty development program focused on VLSI Design. The inauguration ceremony was graced by the presence of Dr. S. Geethalakshmi, the Vice Chancellor, who emphasized the significance of VLSI in computing technology. Dr. V. Cyrilraj, Additional Registrar (Academic), underscored the importance of semiconductor fabrication in India, while Dr. N. Ethiraj, Dean of Engineering and Technology, provided an extensive overview of the manufacturing phases spanning the last three decades.

The welcome address was delivered by Dr. U. Jayalatsumi, Head of the ECE Department, and the guest of honor, Dr. Ushaa Eswaran, Principal of Sri Indira Institute of Science and Technology, was introduced by Dr. M. Janakirani, Professor in the ECE Department. Dr. Ushaa Eswaran, in her presentation, covered various aspects of VLSI Design and highlighted pedagogical initiatives such as open-ended questions, puzzles, and case study experiments. She emphasized the essential topics for aspiring VLSI Design Engineers.

The organization of the program was spearheaded by Dr. Chunchu Rambabu, Professor in ECE, and Mr. P. Jaisankar, Assistant Professor. Dr. S. Deborah, Assistant Professor in ECE, moderated the event, and the proceedings concluded with a Vote of

Thanks delivered by Mr. N. Lakshminarayanan, Assistant Professor in ECE. The Department expressed wholehearted gratitude to the Honorable President for unwavering support and extended appreciation to all executives for their continuous encouragement in orchestrating the successful event.

Day 2: Basics of Consistent Functionality across PVT in IC's

On the second day of the session, Ms. Meghana was the featured guest, introduced initially by Dr. Janaki Rani. Ms. Meghana, the chief guest, delved into the fundamentals of consistent functionality across Process, Voltage, and Temperature (PVT) in Integrated Circuits (ICs). Her presentation covered various aspects, including circuit fabrication, processing speed, and read and writes operations. She emphasized the significance of fabrication in current technology and discussed existing Very Large Scale Integration (VLSI) design, industrial base standards for fabrication, and strategies to address power consumption.

The session proceeded to a detailed exploration of basic Dynamic Random-Access Memory (DRAM) memory cells, particularly focusing on the intricacies of read and write operations, activation commands, and row and column addresses, with specific attention given to 16GB memory. Ms. Meghana also delved into the distinctions between schematics and ICs, covering aspects such as electrical design schematics and physical design layout.

Furthermore, she provided insights into SpFC (Standard Performance Factor of Cell) and SPF (Standard Performance Factor) of physical design. The discussion encompassed routing issues, critical nodes, floor planning, Process, Voltage, and Temperature (PVT) estimation, reliability concerns, and characterization.

Ms. Meghana then turned her attention to compensation techniques in analog circuits, specifically addressing processes, voltage fluctuations, and temperature variations, illustrating these concepts with practical examples.

In the final segment, she elucidated the intricacies of latching test mode trims in analog circuits, providing a comprehensive overview of this essential aspect of circuitry.

Day 3: Heterogeneous Integration

On the third day of the session, Dr. Cyril Prasanna Raj, the esteemed Director (CCCIR), took the stage as the distinguished guest speaker. Dr. Jayalatsumi, the Head of the Electronics and Communication Engineering (ECE) Department, introduced him to the audience. The focal point of the session was Heterogeneous Integration, a cutting-edge topic in the field of electronics and chip design.

Dr. Raj commenced the session by delving into the intricacies of heterogeneous components within integrated circuits. He elucidated on key elements, notably, CPU-GPU Integration, the integration of Accelerators and Coprocessors, the utilization of Diverse Memory Types, and the broad spectrum of Applications within Heterogeneous Chip Design. This comprehensive overview served as a foundation for understanding the amalgamation of various specialized components within single chip architecture.

The discourse smoothly transitioned into the domain of VLSI (Very Large-Scale

Integration) chip design, expanding the discussion to the intricate details of designing highly complex integrated circuits. Dr. Cyril Prasanna Raj shared insights into the nuances of VLSI, shedding light on the methods, challenges, and advancements in this evolving field.

In the latter part of the session, the focus shifted towards practical applications. Dr. Raj expounded on intriguing use cases, notably, the application of VLSI in Micro Air Vehicles—underscoring the practical implications of advanced chip design in emerging technologies. Additionally, he explored the fascinating realm of designing Bio-Inspired models based on integrated circuits, showcasing the interdisciplinary nature of modern chip design and its intersection with biologically inspired engineering.

The session, enriched with valuable insights and real-world applications, provided attendees with a holistic understanding of Heterogeneous Integration, VLSI chip design, and their transformative impact on diverse technological domains. Dr. Cyril Prasanna Raj's expertise and engaging presentation style contributed to a dynamic and informative session that left the audience with a deeper appreciation for the complexities and possibilities inherent in contemporary chip design.

Day 4: Static Timing Analysis on SoC

The session speaker on day-4 of the virtual FDP was Mr. Ravi Sharma, Engineer with Qualcomm India Pvt. Ltd., also a proud Alumnus of our department. The session was on “Static timing analysis on SoC”. He detailed the aspects of IP based design with priority on the tradeoff between less area, high speed and low power consumption. Also the discussion extended to the merits and limitations of static timing analysis with examples of flip-flop and also the availability of Cadence tools for the same. The session ended with enthusiastic participation from the audience through queries and the same was answered well by the session speaker. Mr. N. Lakshminarayanan proposed a vote of thanks. The Department of ECE profusely thank our Management and all Executives for the smooth conduct of the event..

Day 5: Low Power VLSI Techniques

On the fifth day of the session, Dr. S.B. Mohan took center stage as the featured guest, introduced by Dr. K.S. Thivya. During his presentation, Dr. Mohan provided a concise recap of NMOS and PMOS circuits, delving into their characteristics, different modes, and presenting a thorough examination of their advantages and disadvantages.

The session then progressed to an in-depth exploration of designing, synthesizing, and optimizing low-power VLSI circuits. Dr. Mohan offered valuable insights into CMOS logic circuits, drawing comparisons with NMOS and PMOS circuits.

In the concluding segment of his presentation, Dr. Mohan elucidated the intricacies of MOS dynamic circuits and static circuits. He placed special emphasis on the concept of ratioed logic circuits, rounding out the comprehensive coverage of various aspects of VLSI circuitry.

Day 6: Stress Management

Behaviour therapist and Re-Dok Healing Centre founder Dr. T. Anupama presented her talk on stress management on the final day of the faculty development programme on VLSI design. Dr. Manonmani made the guest speaker's introduction.

As there is no one-size-fits-all approach to stress management, the speaker started by emphasising the importance of stress management and its critical role in each of our lives. Dr. Anupama then went into details of several methods of managing stress, such as exercising frequently, performing yoga, doing breathing exercises, maintaining a balanced diet, and living a healthy lifestyle.

She additionally touched on some strategies for handling difficult circumstances with coworkers, at home, and at the office.

The session proved to be quite beneficial for all attendees, as stress management strategies may enhance all aspects of our lives, including our relationships, career, and health.

EVENT OUTCOME

The participants had a wider understanding on various aspects of VLSI Design and highlighted various aspects, including circuit fabrication, processing speed, and read and writes operations and also included Heterogeneous Integration, a cutting-edge topic in the field of electronics and chip design

PHOTOS

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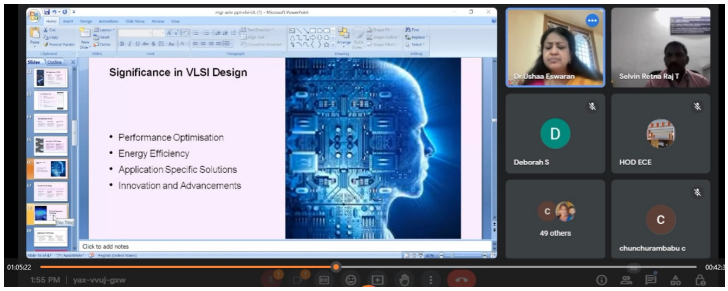

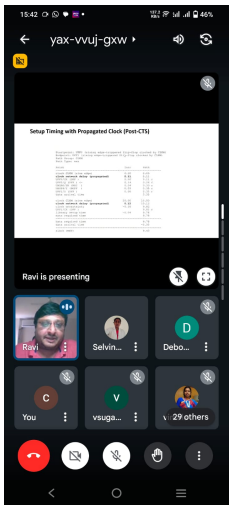

Dr.Rambabu/ Mr.Jaisankar